CURRICULUM-VIATE

Bijender Kumar

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Summary:

Research Potential: I am having extensive research experience (6 years) in Advanced Battery Management System, a chip/FPGA-based design solution for critical health conditioning of a rechargeable battery using soft computing techniques (Neuro-Fuzzy and Statistical Approaches). I have tested and monitored the runtime capacity of many rechargeable batteries for their better operations and performances in electric derive vehicles (EVs, HEVs and plug-in HEVs). I have designed a FPGA hardware implementing the Advanced BMS for combined and accurate estimation of SOC & SOH of a rechargeable battery. My research area is extended to BMS Design, FPGA/ASIC/DSP design, Battery SoC & SoH Monitoring algorithms, ANN controller and fuzzy logic controller, but not limited.

Teaching Potential: I am also having extensive teaching experience (10 years) in different reputed engineering institutes and universities of INDIA. I have taught almost all subjects of B.Tech (Electronics/Electrical Engineering) and M.Tech (Electronics/Electrical Engineering) courses, especially VLSI Design, DSD, AEC, ESD, MOS ICs, DE, AE, EDC and BOE etc. I have achieved lot of appreciation and respect from employer as well from my students, during my teaching carrier. I have also been the research guide of many M.Tech students for supervising their research work.

I always wish to obtain a long-term career with those organizations, which believe in the enhancements of the personal, society & professionals. And where I can contribute to their progress using my research, academics & administrative skills and where my skills get honed.

Educational Qualifications:

Degree	University/College	Passing Year	%age
Ph.D (Electronics Engg.)	Banasthali University, Rajasthan	2017	Submitted
M.Tech.(Microelectronics & VLSI Design)	K.U. Kurukshetra	2007	75%
M.Sc. (Electronics)	K.U. Kurukshetra	2004	62%
B.Sc. (Electronics)	M.D.U. Rohtak	2002	70%

Employment History: 11 (approx.) years experience in research & academics

Head of Department (ECE) & Asst. Professor — August 2010 – Till Date
Gurgaon Institute of Technology & Management, Bilaspur Tauru Road, NH-8, Gurgaon, HARYANA (INDIA)

Head of Department (ECE) & Asst. Professor — July 2008 – August 2010
World Institute of Technology,
Sohna Palwal Road, Sohna, Gurgaon, HARYANA (INDIA)

Lecturer (ECE) — May 2007 – July 2008
Gurgaon Institute of Technology & Management, Bilaspur Tauru Road, NH-8, Gurgaon, HARYANA (INDIA)

Firmware Engineer — One Year (2004-2005)
WebCom Technology Pvt. Ltd.
South Ex-II, New Delhi

Trainee Engineer — One year (6 months + 6 Months)
HCL Technology Pvt. Ltd, Noida, U.P. (INDIA)

Technical Skills:

* **Programming Languages:** VHDL, Verilog, MATLAB, SPICE, C and assembly languages for 8085 & 8086 (Microprocessors) and 8051 (Microcontroller).

* **Tools/Packages:** Xilinx ISE series, Model Sim , MATLAB Simulink , uartus II .., Altera Max plus II, Active HDL, Project Navigator, Tanner Tool, Silvaco, Keil, Circuit Maker and Leonardo Spectrum.

Operating System: DOS, Windows, UNIX Elementary.

Research Work:

Ph.D Research: "Mixed Signal FPGA Design of Advanced Battery Management System".

Organization: Banasthali University, Rajasthan

Description: My Ph.D research work attempted a chip FPGA based solution of an Advanced Battery Management System BMS for combined and accurate monitoring of SOC & SOH of a battery used in electric derive vehicles. Smooth functioning of heavy mobile systems depends on the accurate SOC and SOH monitoring. The monitoring is addressed by an independent system known as BMS. BMS has been the essential integral part of all electric derive vehicles and provides safety to the system as well as to user with run time monitoring of battery state for any critical hazarder conditions. The accuracy of these systems for charge and health monitoring has always been a great challenge for engineers & researchers. In my Ph.D research, I have used MATLAB to FPGA design methodology for Advanced BMS chip implementation. The FPGA implementation of Advanced BMS includes Neural Network Controller NNC, Fuzzy Logic Controller FLC & Statistical Model. The battery parameters required to design the Advanced BMS are extracted from the experimental results and incorporated in development of Advanced BMS model. The Neuro Fuzzy approach NNC & FLC together is used to model the electrochemical behavior of the Lead acid battery then used to estimate the SOC of the battery. The Statistical model is used to address *battery's SO*H. The Advanced BMS simulation and synthesis results are validated by experimental results and found very satisfactory. The adopted approach & developed architecture of Advanced BMS provides more than accuracy in SOC estimation and reasonably accurate SOH.

The developed FPGA design of Advanced BMS has advantages over other existing BMS because of low non recurring engineering NRE cost, low power consumption, high speed of operation, large reconfigurable logic, large data storage capacity, more flexible interfaces and hence better performance.

 # M.Tech Research – "Design and Simulation of Memory BIST using VHDL"

Organization: HCL Technology Pvt. Ltd. Noida

Description: The objective of this project was to design and simulation of memory BIST architecture with better fault coverage and high speed of testing. BIST Architecture was designed with blocks, like Test generation, controller and comparator with CUT, as its major modules. The controller is basically is a FSM which has 16 states according to March-M (16n) algorithm and 8 states according to March-Y (8n) algorithm.

 # M.Sc– "Design and simulation of floating point unit – FPU using VHDL"

Organization: HCL Technology Pvt. Ltd. Noida

Description: The objective of this project was to design and simulation of FPU dedicated for Floating-Point Processors. FPU was dedicated to perform the arithmetic & logical operations on the floating point operands which can easily be incorporated in any general purpose processor. In this project, the RTL code was written and then implemented on FPGA for verifying the results.

 # Industrial research – "Design of Hardware Protection and Security Device (HPSD)/Dongle"

Organization: WebCom Technology, South Ext. New Delhi.

Description: The objective of this project was to save the costly software from piracy. In this, a key was provided to access the particular software. My task in this project was to write the RTL coding for E2PROM and for algorithms of Cryptography (AES & DES). That was simulated, synthesized and implemented using Sparton-3 Xilinx FPGA.

Research Publications:

S. No.	Title	Author(s)	International Journal/ Conference	Year of Public-ation
1	A VHDL Implementation of Advanced Battery Management System targeting FPGAs http://www.sgem.org/sgemlib/spip.php?article6109&lang=en	Bijender Kumar, Neeta Khare, PK Chaturvedi	**SGEM 2015 Bulgaria** indexing in Thomson Reuters, Elsevier-SCOPUS, ISI Web of Science and Engineering Village/Compendex.	June, 2015

2	Advanced Battery Management System using MATLAB/Simulink http://ieeexplore.ieee.org/document/7572 7/	Bijender Kumar, Neeta Khare, PK Chaturvedi	**IEEE INTELEC 2015 at Osaka, Japan.**	October, 2015
3	FPGA Design Scheme for Battery SOC SOH Algorithms for Advanced BMS	Bijender Kumar, Neeta Khare, PK Chaturvedi	Journal of Energy Storage, Elsevier	Commu- nicated
4	FPGA-based Design of Advanced BMS Implementing SOC & SOH Estimators	Bijender Kumar, Neeta Khare, PK Chaturvedi	Journal of Energy Storage, Elsevier	Commu- nicated
5	Neural Network Controller For Renewable Energy Applications	Bijender Kumar, Jyoti Yadav	National Conference o advances in Mechanical Engineering (NCAME 2014)	2014
6	Designing a Predictive Model for Heart Disease Detection Using Artificial Neura Network	Mr. Bijender Mehandia, Antim Dev Mishra	International Journal o Electrical,Electronic and Mechanical Fundamentals	2013
7	Comparative Analysis of Energy Efficien Mac Protocol for Wireless Sensor Networks	Bijender Mehandia, Manju Yadav	International Journal o Engineering Sciences	2013
8	Automation of CNG and Petrol Switches for Automotive Applications	Raj Kumar, BijenderKumar, Parmender, Bharti Gupta	International Journal for Scientific Research & Development	2013
9	Resource Allocation in Multiuser OFDM	Mr. Bijender Mehandia, Devender Kumar	International Journal o Electrical, Electronics and Mechanical Fundamentals	2013
10	Floating Point Unit Implementation on Sparton 3E FPGA	Bijender M'dia,Deepa Saini	journal	2012
11	Implementation of Sine & Cosine using Volder's CORDIC Algorithm	Mr. Bijender Mehandia, Mr. Jitender Chhabra	journal	2012
12	A CenterElimination Approach to Resolve Congestion in Optical Grid Network	Bijender Mehandia,Manoj Kumar	journal	2012
13	Effect Of Channel Doping, Concentration And SOI Layer Thickness on Electrical Behaviorof SOI MOSFET Using Silvaco TCAD Simulator	Bijender Mehandia, Sapna	journal	2012

14	Design & Simulation of A Low Power Content Addressable Memory□CAM□ Cell	Bi□ender Kumar, Sumit Rani	National Conference on Emerging Trends in Science, Technology & Management□Vision □□□□	□□□□
15	Prediction of Heart Attack Using Artificial Neural Network	Bi□ender Kumar, Antim Dev Mishra, Rakesh Kumar	National Conference on Emerging Trends in Science, Technology & Management□Vision □□□□	□□□□
16	Comparison of Singlehop and Multihop Communication in Wireless Sensor Networks	Bi□ender Kumar, Man□u □adav	National Conference on advances in Mechanical Engineering □NCAME□ □□□□□	□□□□

Administrative Assignments:

- All Administrative tasks as the Head of Department
- AICTE□UGC□University Work
- Branch Counselor of IEEE student branch
- Head of International Tech Fest IGNITRON□□under IEEE student branch
- Co□convener of different national conferences
- Member of research papers selection committee
- University examination papers setting
- Academic Program Supervision
- Academic Advisor for different institutes
- Pro□ect & Thesis adviser for M.Tech □ECE□ students
- Research Consultant for different companies like Incise Infotech, Xinoe Systems & DKOP labs

Other Academic/Research Achievements:

- *Reviewed one research paper "State□of□charge observers for lead□acid storage units used in autonomous solar applications"* EST□□□□□□□□□□**Journal of Energy Storage, Elsevier.**
- Dale Carnegie certified on a mission□□Xworkshop on **"High Impact Teaching Skills"** from WIPRO.

- Appreciation certificate from the Director GITM on grand success of International Tech Fest IGNITRON under IEEE Student Society.
- Best Teacher award at GITM, Gurgaon.
- Appointed as oint Secretary to organize **NASET (National Level Symposium on Electronics Technology)** during M.Sc. for the year , organized by IEEE and Electronics Society.
- Member of organization committee in **IMS (Indian Microelectronics Society)** conference held at Kurukshetra University during M.Tech, in .
- Guided a M.Sc. GIS student of ITC, Netherland & SRO Remote Sensing Lab, Dehradun and the four students outside GITM of M.Sc. Electronics & one M.Tech VLSI student from Banashthali Vidyapeeth, Ra asthan.

Workshop/Seminar/Conferences:

- Attended workshop on "Teaching with MATLAB and Simulink" at S.V. National Institute of Technology, Surat.
- Seminar delivered on "VLSI Design Flow" in Faculty Development program at GITM.
- Attended workshop on "VLSI Design & CAD Tool" at NIT Hamirpur.
- Attended Power Grid international conference at Pargati Maidaan, New Delhi.
- Attended Seminar cum Workshop on "Embedded Systems & VLSI design" organized by Xinoe Systems Pvt. Ltd.
- Head organizer of "MATHLAB – BOTRIX" Workshop organized by IIT Bombay at GITM.
- Attended Seminar cum Workshop on "FPGA Design Using Xilinx" organized by DKOP Labs Pvt Ltd. at GITM.

Personal Profile:

Name	Bi ender Kumar
Date of Birth	th April
Marital Status	Married
Language Known	English, Hindi
Strengths	Good Facilitator, Fast Learner and Hard Worker

References:

Dr. Neeta Khare
Senior Development Scientist
The Energy Storage Research Centre ESReC
Switzerland
Email: neeta_ks@yahoo.com

Dr. P.K. Chaturvedi
Professor, ECE
SRM University
Ghaziabad, U.P. INDIA
Email: pkchat1945@gmail.com

I hereby declare that information given above is true as the best of my knowledge.

Date:

Place: **(Bijender Kumar)**